Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A0**
2. **EN**
3. **V-**
4. **S1**
5. **S2**
6. **S3**
7. **S4**
8. **D**
9. **S8**
10. **S7**
11. **S6**
12. **S5**
13. **V+**
14. **GND**
15. **A2**
16. **A1**

**.093”**

**14 15 16 1 2**

**10**

**11**

**12**

**13**

**9 8**

**7**

**6**

**5**

**4**

**3**

**AG41Z**

**MASK**

**REF**

**.119”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0045 x .0045”**

**Backside Potential:**

**Mask Ref: AG41Z**

**APPROVED BY: DK DIE SIZE .093” X .119 DATE: 9/23/21**

**MFG: MAXIM THICKNESS .014” P/N: DG508A**

**DG 10.1.2**

#### Rev B, 7/1